IMPROVED DEVICE MODELING FOR MATCHING NETWORK SYNTHESIS

Max W. Medley, Jr., Senior Member, IEEE
TRAK Microwave Corporation
Tampa, Florida
and
J. Lamar Allen, Fellow, IEEE
University of South Florida
Tampa, Florida

ABSTRACT

A new technique is presented for determining equivalent source and load device models applicable to GaAs FET or other devices for which measured data is available. The new technique provides a more accurate starting point for matching network synthesis, better prediction of achievable circuit performance, and does not require the unilateral device assumption. Simple computer optimization and elements with negative reactance slope parameters are utilized. A description of the method and an example of its application to GaAs FET amplifier design is presented.

Introduction

Advances in the performance of microwave devices and the ever increasing demands on system requirements have progressed to the point where designers must be able to obtain near optimum performance from active devices, and certainly must be able to accurately predict the maximum obtainable circuit performance for practical matching networks. Computer optimization has proven to be of enormous benefit since several "known to be practical" matching networks may be optimized in the hope of finding one for which fabrication requirements are reasonable and acceptable performance is obtained. A desirable refinement of the usual optimization technique is to use an equivalent source and load model for the device, and from network synthesis define the matching network and a starting set of element values. The overall structure is then optimized. Such procedures require no apriori knowledge of the matching network.

Techniques necessary to synthesize distributed matching networks in a variety of forms are readily available, as are techniques used to determine gain-bandwidth limitations for a given device model. The term "device model" is actually a misnomer when used with multiport matching network synthesis since no attempt is made to completely model a particular device. Instead, an equivalent complex impedance is determined for each port of the device such that any network designed to match into the complex load can also be connected to the appropriate device port with similar results. This artifice enables the gain-bandwidth limitations to be determined for various orders of matching networks, which immediately defines the number of sections, ripple, and minimum insertion loss which must be accepted. The complex load also determines the termination resistance at one end of the synthesized network as well as the value and type of the first element since this portion of the network is actually the complex load.

Present procedures used to generate the device models are not accurate and/or complete enough to always permit adequate matching networks to be designed. Most existing modeling techniques assume a unilateral device, and derive the equivalent model from S_{11} and S_{22}, or if noise figure is an important factor, an equivalent circuit which tracks the optimum noise impedance may be substituted for the input portion of the model. The unilateral assumption is certainly not reasonable at higher microwave frequencies, and at lower frequencies a match to S_{11} and S_{22} can very well lead to the design of an oscillator rather than the intended amplifier. Another disadvantage of existing techniques, even when some refinement is made to account for the bilateral case, is that reactive gain slope compensation is usually required, and although not difficult to synthesize, the load and source impedances which result cannot be predetermined. An appropriate selective mismatch can frequently be used to lower VSWR, stabilize the circuit, provide a lower noise figure, or higher output power.

A technique using "negative image" equivalent circuits and simple computer optimization has been developed for deriving equivalent source and load models for GaAs FETs and other devices. This technique allows device models to be derived from measured bilateral S-parameters, as well as from noise and power data. The error function can be weighted in the usual manner for circuit optimization to produce the most desirable compromise between VSWR, gain, noise figure, output power, and stability. Gain-bandwidth limitation of the models can easily be included in the error function, and restrictions imposed on the resulting models to ensure that the order of the required synthesized matching network will be practical.

Device Modeling

The concept of negative image equivalent source and load networks is developed in the following paragraphs. If one were given source and load models of a device, "hypothetical" networks which would exactly match the given models at all frequencies could be generated as the topographical image of the models with all model element values replaced by corresponding negative values. That such "negative image" networks provide the desired match is easily shown in the S plane using the ABCD transmission matrix, where S is either the complex frequency variable, $\sigma + j\omega$, for lumped element networks, or Richards' variable, $\Sigma + j \tan \beta l$, for distributed elements. When any element is cascaded with an identical but negative counterpart, the result is the identity matrix, which indicates perfect transmission, independent of frequency. Since matrix multiplication is associative, the two matrices which correspond to the positive element for the device model and the adjacent negative element of the matching network can be multiplied together to form the identity matrix, then eliminated, which again results in two adjacent positive and negative elements which can be eliminated, with as many repetitions as required.

In practice, the source and load device models are not usually known but are rather "to be determined." The desired models can be obtained from the measured device parameters using the inverse of the above procedure. Moreover, the models can easily be constrained to reflect desired overall performance characteristics such as minimum noise figure. First, a "likely" structure and trial element values for the hypothetical source and load negative image matching networks are deduced from Immittance Plane plots of measured device data. Next, the hypothetical networks are combined with the device (characterized by measured data) as shown in Figure 1.

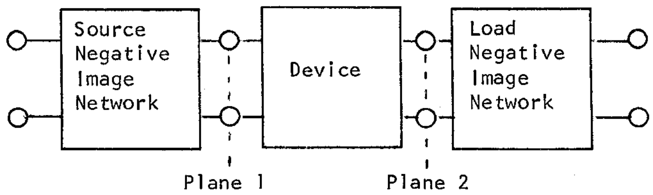

Figure 1: Device characterization by negative image networks.

Any desired performance constraints are now applied to the port characteristics of the combined structure via a computer optimization routine in which the variables are the element values of the hypothetical networks. The output of the preceding step is a pair of optimized hypothetical networks which, in combination with the actual device, produce the overall specified gain, noise figure and/or other port constraints. Finally, the negative image looking to the left at plane 1 is the device source model under the imposed constraints. Likewise, the negative image looking to the right at plane 2 is the device load model under the imposed constraints. These models are very accurate and contain no apriori limitations such as the unilateral device assumption.

The optimization required in the modeling process proceeds very rapidly since the number of variables is typically small. The computer program must be able to handle negative element values. Gain-bandwidth limitation[1,2] or minimum insertion loss and ripple, can be computed for each iteration of the models and used as a portion of the error function to ensure that the desired performance will be met with realizable synthesized networks based on the optimized models. The required matching networks are thus synthesized with the derived highly accurate source and load device models as terminations.

Amplifier Design

The design of a 2.0 to 4.0 GHz amplifier will be used to illustrate this design technique. The design goals will be 10 dB gain, with less than 2.5 dB noise figure across the band. The Hewlett Packard HFET-1101 will be used since detailed data for both noise figure and S-parameters is available. Figure 2 shows the gain, noise figure, and stability contours mapped on the source plane. These contours indicate that there will be a problem achieving 10 dB gain and 2.5 dB noise figure at the low end of the band assuming a good output match; however, the gain on the source plane can be increased which will cause the constant gain contour to fall inside the 2.5 dB noise figure circle. If this approach is taken, mismatch circles must be constructed on the output plane to compensate for the increase in low end gain. The type of model network can be determined directly from the source and load mappings since these represent the impedance that must be presented to the device, or the impedance seen looking into the negative image networks. In the case of the input, a positive series reactance is required which decreases with frequency. A series-connected open stub with a negative characteristic impedance in series with a resistor will meet this requirement.

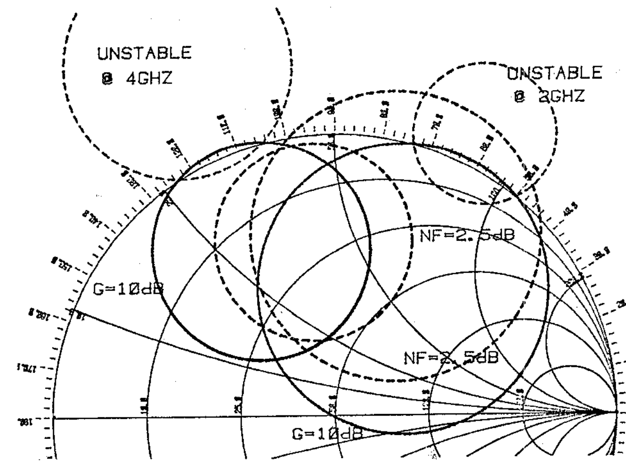

Figure 2: HFET-1101 Source Plane

An approximate value for the stub can be determined by assuming a characteristic impedance, and calculating the electrical length at some frequency. The initial values selected for the source negative image network are 30 ohms in series with an open stub with characteristic impedance of -50 ohms and electrical length of 40° at 4.0 GHz. The output model is determined in the same manner using either mismatch contours, or $S_{22}'^*$. Since the 10 dB gain contours were used to define the input model, the output must be matched, or the output network should present $S_{22}'^*$ to the device. The negative image output model is a parallel combination of 125 ohms and an open stub of -50 ohms and 32 electrical degrees at 4.0 GHz. A schematic representation of the computer model to be optimized is given in Figure 3.

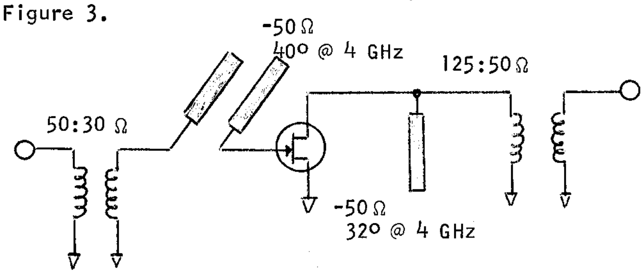

Figure 3: Computer Model

The input and output negative image network values are now optimized for the desired performance specification using a computer-aided design program. The resulting optimized source and load device models are given in Figures 4a and 5a, respectively. The overall optimized performance using the ideal negative image networks is 10 ± 0.15 dB, and a maximum noise figure of 2.8 dB at the low end of the band. The gain-bandwidth limitation on the input network is far greater than that of the output; therefore, the input matching network will be synthesized and then optimized while the output remains in the image model form. This approach increases the optimization speed since fewer variables are required.

Several distributed synthesis procedures are useful for the matching network design. Levy's technique[3] for impedance transforming filters and the work of Mokari-Bolhasson and Ku[4] have been incorporated in a minicomputer based synthesis program. The technique of [4] has been modified to allow for the synthesis of generalized structures with specified commensurate line length. Several networks can easily be investigated for physical realizability and the desired termination impedance. In some cases, partial element extraction can also be used to adjust the termination impedance.

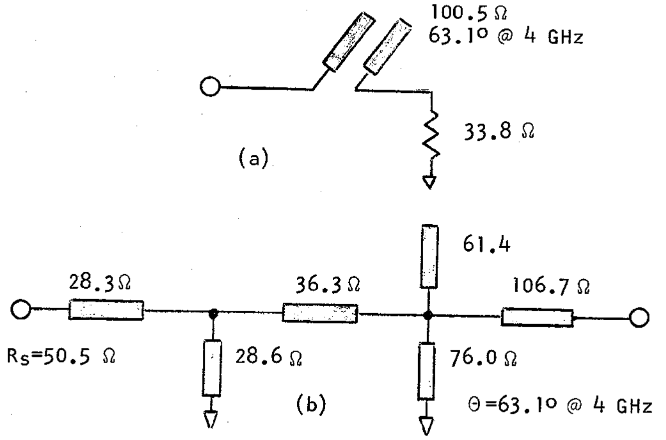

Figure 4: (a) Optimized input model. (b) Synthesized input network.

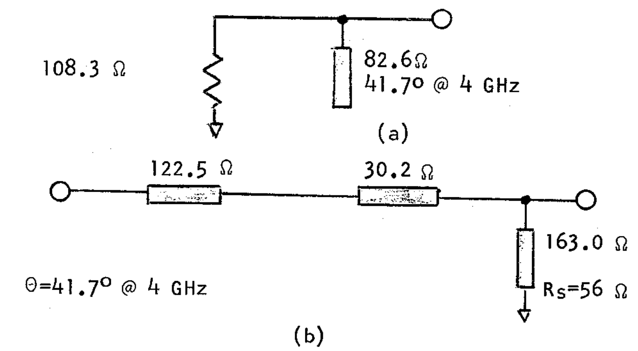

Figure 5: (a) Optimized output model. (b) Synthesized output network.

Based on the optimized input model (shown in Figure 4a), a network with two transmission line elements, one low-pass element, and three high-pass elements was synthesized for 0.3 dB Chebyshev ripple and 0.87 dB minimum insertion loss. Partial element extraction was used to adjust the termination impedance to 50.5 ohms, and a non-minimum transmission line element was extracted to allow easier physical realization. Many other networks may be synthesized to match to this source device model. The network shown in Figure 4b is quite satisfactory since the element values are realizable and the structure has a shorted stub which can be used to ground the FET gate.

Optimization of the distributed structure provides improved performance over the synthesized network since an additional degree of freedom is added when the line length in allowed vary. The results from the optimization of input matching network and output negative image model meets all the performance specifications, the gain is exactly 10.0 dB and the maximum noise figure is 2.4 dB at 2.0 GHz. The output model resulting from this process is shown in Figure 5 along with the synthesized matching network. This network has 0.05 dB Chebyshev ripple and zero minimum insertion loss with a termination impedance of 56 ohms.

The final optimized circuit is shown in Figure 6.

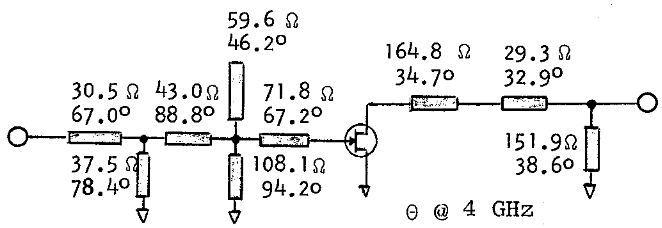

Figure 6: Final Amplifier Circuit.

The performance which is obtained from this design is 10.0 ± 0.3 dB gain with a noise figure of less than 2.3 dB across the 2.0 to 4.0 GHz band. The next step should be to constrain the impedance values to realizable levels and again optimize using a constrained search. This will not effect the performance to any significant degree since the element values which may be difficult to realize are in the output network which has a high gain-bandwidth product. The final step involves modeling all parasitics and losses which can be identified, and perform one last optimization on only those variables which do not effect the parasitic values.

Conclusion

A technique for deriving highly accurate source and load device models from measured device data has been described. The technique which is based on "negative image" networks does not require a unilateral device assumption and constraints representing a compromise of several device characteristics can easily be imposed. An application of the negative image modeling technique to the design of a microwave amplifier has been illustrated.

References

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